Analog Interview Questions

By

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1. State whether True or False

   a) Electro migration depends on current.

   b) In LOCOS selective oxide growth is achieved using Silicon dioxide.

   c) CVD process does not consume underlying silicon

2. To remove antenna effect which method is used

   (i) Metal Splitting (ii) Putting Antenna diode (iii) Metal Slotting (iv) Metal Over Etching

   (a) (i) and (iii) are true

   (b) (i) and (ii) are true

   (c) (i) (ii) and (iii) are true

   (d) (ii) and (iv) are true

3. In an Inverter circuit if the following condition lies for input voltage

   Vin = Vdd/2 then

   (a) n-mos will be in cut off and p-mos will be in linear region

   (b) n-mos will be in linear and p-mos will be in cut off region

   (c) n-mos and p-mos both will be in cut off region

   (d) None of these

4) Calculate Rz? (Two NMOS are connected in diagram shown below)

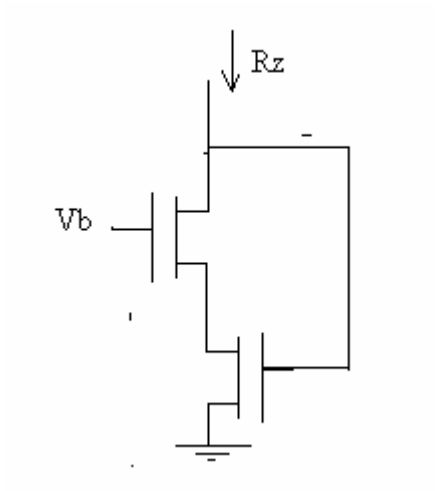


Figure 1

5) If Vg1 is fixed to 2.5V and Vg2 is sweep from 0 to 5V, Draw Vout waveform (assume VDD = 5V)

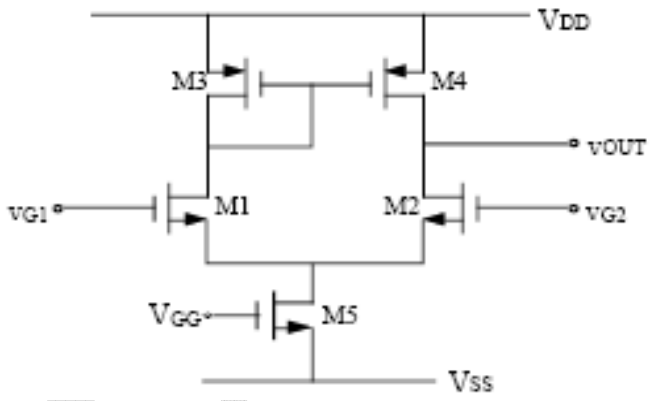


Figure 2

6) Assume threshold voltage of PMOS is –Vt & NMOS is Vt , a input pulse from VSS to VDD is given to circuit shov below, Draw the output waveform

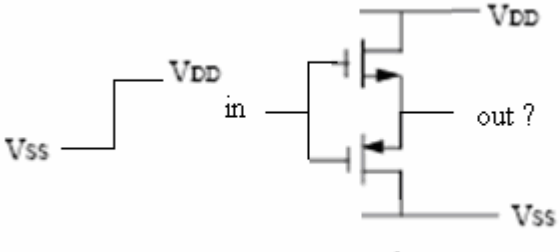
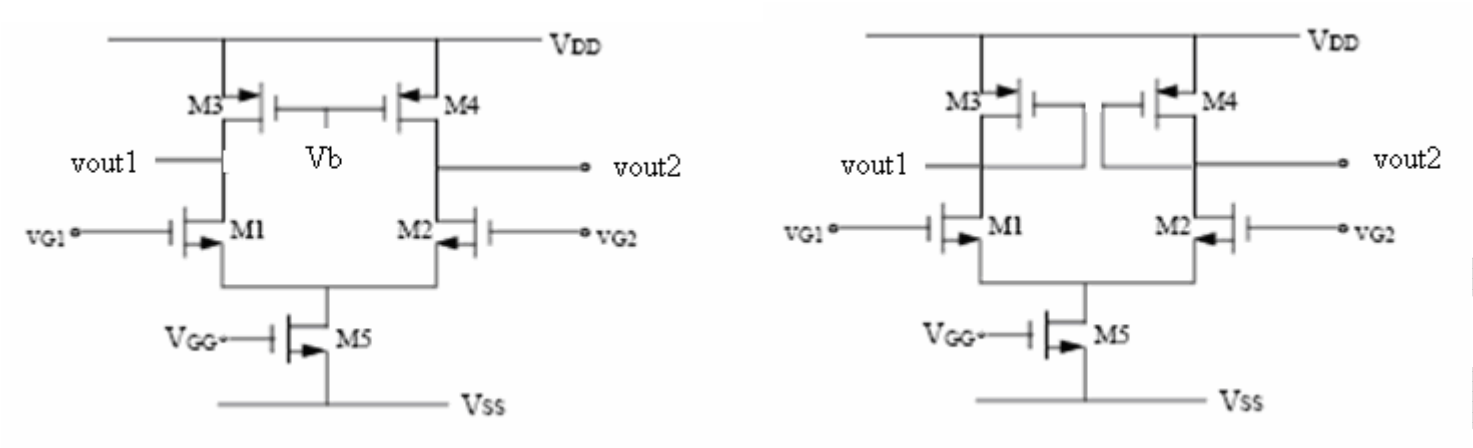
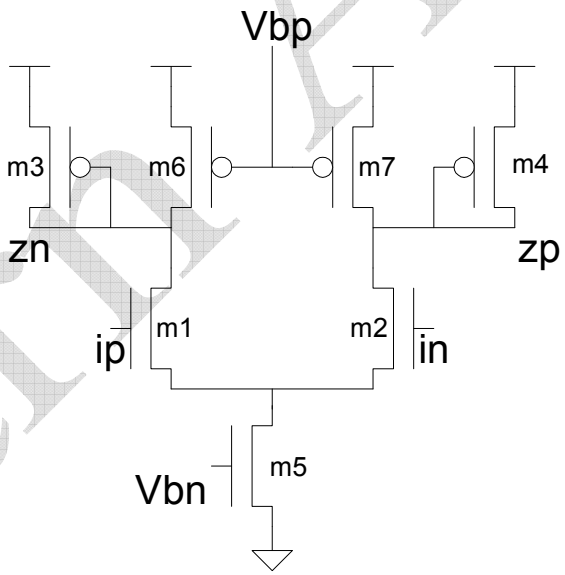


Figure 3



(Figure 4)

9) Tell me the advantages of amplifier shown in figure 5 over those shown in figure 4 ?



(Figure 5)

10) What is a miller compensation technique?

11) Draw an OPAMP & tell me various poles & zeros associated with the circuit you draw ? How you will stabilize yo system?

14) What are main advantages of making CMOS circuits working in sub threshold regions?

15) Describe Electro migration effect? & ways to reduce Electro migration during layouts?

16) What is CMP dishing? How metal slotting & dummy metal help in reducing CMP dishing ?

17) Describe OPC techniques & phase shift mask?

18) What is Latch up? Tell me at least 5 ways how we can reduce probability of a latchup in ur circuit ?

19) Draw the layout of M1 & M2 transistor in figure 5 (hint : - take care of Matching pattern , Match routing & guard r etc) .

20) how you can match you resistor & capacitor layouts ?

21) what are advantages of Common centroid & interdigitized patterns

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